In the Claims:

1. (Canceled)

2. (Previously Presented) A method for activating a deactivated frequency synthesizer comprising:

activating a voltage controlled oscillator;

allowing the voltage controlled oscillator to stabilize;

configuring a main frequency divider of the synthesizer to operate as it had prior to deactivation of the synthesizer; and

activating the main frequency divider.

3. (Original) The method of claim 2 further comprising:

deactivating a phase frequency detector prior to activating the main frequency divider; and

activating the phase frequency detector after the main frequency divider is activated.

4. (Previously Presented) The method of claim 2 further comprising:

configuring a reference frequency divider of the synthesizer to operate as it had prior to deactivation of the synthesizer.

5. (Previously Presented) The method of claim 3 further comprising:

activating a reference frequency divider.

6. (Original) The method of claim 5 wherein the main frequency divider is activated so that a signal from the reference frequency divider initially reaches the phase frequency detector before a signal from the main frequency divider.

7. (Previously Presented) The method of claim 5 wherein the main frequency divider is activated such that the phase of a signal from the main frequency divider initially lags a phase of a signal from the reference frequency divider at the phase frequency detector.

8. (Currently Amended) The method of claim 2 further comprising:

tuning the voltage controlled oscillator to the frequency the ~~radio device~~ synthesizer had operated at before being deactivated.

9. (Previously Presented) The method of claim 8 wherein tuning the voltage controlled oscillator includes

receiving an initial voltage signal stored in a capacitive device corresponding to the operating frequency the synthesizer had operated at before being deactivated.

10. (Original) The method of claim 2 further comprising:

tuning the voltage controlled oscillator to the new desired operating frequency.

11. (Currently Amended) The method of claim 10 wherein the time in between ~~receiving the external signal~~ activating the voltage controlled oscillator and tuning the voltage controlled oscillator to the new desired operating frequency is less than or equal to two hundred micro-seconds.

12-19. (Canceled)

20. (Original) A method for activating a synthesizer comprising:

activating a synthesizer voltage controlled oscillator;

activating a main frequency divider such that it is initially out of phase with a reference frequency divider; and

activating a phase frequency detector after the main frequency divider is activated to receive input signals from the reference frequency divider and the main frequency divider.

21. (Previously Presented) The method of claim 20 for activating a synthesizer wherein the main frequency divider is activated such that its output signal initially lags a phase of an output signal from the reference frequency divider by a known phase difference.

22. (Previously Presented) The method of claim 20 for activating a synthesizer wherein the

phase frequency detector provides a phase-error signal corresponding to the difference between the phases of output signals from the main frequency divider and reference frequency divider.

23. (Previously Presented) The method of claim 22 for activating a synthesizer wherein the phase-error signal from the phase frequency detector causes the main frequency divider to shift the phase of its output signal to the phase frequency detector.

24. (Original) The method of claim 23 for activating a synthesizer wherein the main frequency divider shifts the phase of its output signal by advancing the phase of its output signal.

25. (Previously Presented) A frequency synthesizer comprising:

a phase frequency detector to detect the phase difference between a first input signal and a second input signal and output a corresponding phase-error signal;

a first reference frequency source coupled to the phase frequency detector and to provide a first frequency signal as the first input signal to the phase frequency detector;

a voltage controlled oscillator, coupled to the phase frequency detector to receive the phase-error signal from the phase frequency detector and generate an output signal at a corresponding frequency and phase; and

control logic to activate the synthesizer when a transmission is expected, configured to activate the voltage controlled oscillator, allow the voltage controlled oscillator to stabilize, inhibit the phase frequency detector, enable the first input signal to the phase frequency detector, enable the second input signal to the phase frequency detector, and activate the phase frequency detector.

26. (Original) The synthesizer of claim 25 wherein the phase frequency detector generates the output phase-error signal as a result of phase differences between the first input signal and the second input signal to bring the first input signal and second input signal into phase.

27. (Original) The synthesizer of claim 25 further comprising:

a frequency filter to filter the signal from the phase frequency detector and to maintain a charge corresponding to the DC value of the phase-error signal from the phase frequency

detector when the synthesizer is deactivated.

28. (Original) The synthesizer of claim 27 wherein the frequency filter includes a capacitive element which stores a voltage charge corresponding to the phase-error signal from the phase frequency detector while the synthesizer is deactivated.

29. (Previously Presented) The synthesizer of claim 25 further comprising:

a reference frequency divider coupled to the first reference frequency source to provide the first input signal to the phase frequency detector; and

a main frequency divider coupled to the output of the voltage controlled oscillator and adapted to provide the second input signal to the phase frequency detector.

30. (Original) The synthesizer of claim 29 wherein the reference frequency divider and main frequency divider are counter devices.

31. (Original) The synthesizer of claim 29 wherein the reference frequency divider is configured to provide a desired operating frequency.

32. (Original) The synthesizer of claim 29 wherein the main frequency divider is configured to provide a desired operating frequency.

33. (Previously Presented) The synthesizer of claim 25 wherein the control logic is configured to first activate the synthesizer to a frequency the synthesizer had previously operated at before being deactivated.

34. (Original) The synthesizer of claim 33 wherein the synthesizer is allowed to coarsely tune to its previous operating frequency.

35. (Previously Presented) The synthesizer of claim 34 wherein once the synthesizer is coarsely tuned to its previous operating frequency, the control logic is configured to change the synthesizer frequency to a new desired operating frequency.

36. (Original) The synthesizer of claim 25 wherein just after the phase frequency detector is activated the control logic is configured to cause the first input signal to reach the phase frequency detector before the second input signal.

37. (Original) The synthesizer of claim 25 wherein the phase of the second input signal initially lags the phase of the first input signal by a known phase difference.

38. (Previously Presented) An apparatus comprising:

means for activating a synthesizer device;

means for setting an operating frequency of the synthesizer device to a frequency the synthesizer device had operated at before being deactivated; and

means for setting the operating frequency of the synthesizer device to a new desired operating frequency.

39. (Previously Presented) The apparatus of claim 38 further comprising:

means for activating a voltage controlled oscillator;

means for allowing the voltage controlled oscillator to stabilize;

means for tuning the voltage controlled oscillator to the frequency the synthesizer device had operated at before being deactivated; and

means for tuning the voltage controlled oscillator to the new desired operating frequency.

40. (Previously Presented) The apparatus of claim 38 further comprising:

means for configuring a main frequency divider of the synthesizer device to values it operated at prior to having deactivated the synthesizer device; and

means for activating the main frequency divider.

41. (Previously Presented) The apparatus of claim 40 further comprising:

means for deactivating a phase frequency detector prior to activating the main frequency divider; and

means for activating the phase frequency detector after a reference frequency divider.

42. (Previously Presented) The apparatus of claim 40 further comprising:
means for activating a reference frequency divider.

43. (Original) The apparatus of claim 42 wherein the reference frequency divider is activated before the main frequency divider.

44. (Previously Presented) An apparatus comprising:
means for deactivating a phase frequency detector;
means for providing a first signal to the phase frequency detector;
means for providing a second signal to the phase frequency detector such that a phase of the second signal initially lags a phase of the first signal; and
means for activating the phase frequency detector.

45. (Original) The apparatus of claim 44 further comprising:
means for providing a carrier frequency at a desired frequency.

46. (Previously Presented) The apparatus of claim 44 further comprising:
means for configuring the means for providing a first signal to provide a signal corresponding to a desired frequency.

47. (Original) The apparatus of claim 44 further comprising:
means for configuring the means for providing a second signal to provide a signal corresponding to a desired frequency.

48. (Currently Amended) A method for conserving power comprising:
deactivating a synthesizer while not in use;
activating the synthesizer, including
configuring a main frequency divider to operate at a first desired frequency;
providing a reference signal to a phase frequency detector; and
activating the main frequency divider to provide an output signal to a the phase

frequency detector, a phase of the output signal lagging a phase of the reference signal to the phase frequency detector.

49. (Previously Presented) The method of claim 48 for conserving power wherein the phase frequency detector provides a phase-error signal corresponding to the difference between the phase of the reference signal and the phase of the output signal from the main frequency divider.

50. (Currently Amended) The method of claim 49 for conserving power further comprising:

providing the phase-error signal to a voltage controlled oscillator such that the voltage ~~control~~ controlled oscillator provides an operating frequency signal for the synthesizer at the desired frequency.

51. (Previously Presented) The method of claim 50 for conserving power wherein deactivating the synthesizer when not in use includes

deactivating the voltage controlled oscillator when the synthesizer is not in use.

52. (Original) The method of claim 51 for conserving power wherein

the synthesizer is not in use when it is not receiving or transmitting.

53. (Previously Presented) The method of claim 48 for conserving power wherein deactivating the synthesizer when not in use includes

deactivating the phase frequency detector when the synthesizer is not in use.

54. (Previously Presented) The method of claim 48 for conserving power wherein deactivating the synthesizer when not in use includes

deactivating the main frequency divider when the synthesizer is not in use.

55. (Previously Presented) The method of claim 48 for conserving power wherein activating the synthesizer includes

activating a voltage controlled oscillator;

configuring a main frequency divider to operate at a frequency it operated at before being

deactivated;

providing a reference signal to a phase frequency detector;

activating the main frequency divider to provide an output signal to a phase frequency detector, a phase of the output signal lagging a phase of the reference signal to the phase frequency detector;

permitting the voltage controlled oscillator to coarsely lock onto the frequency it operated at before being deactivated; and

configuring the main frequency divider to operate at the first desired frequency.

56. (Previously Presented) The method of claim 48 for conserving power wherein activating the synthesizer includes

configuring a reference frequency divider to provide the reference signal to the phase frequency detector corresponding to the desired operating frequency.

57-59. (Canceled)